WHAT IS CLAIMED IS:

1   1.   A memory card, comprising:

2   a first interface controller operable to be

3   coupled to a first interface, said first interface

4   operating to receive database input signals;

5   a second interface controller operable to be

6   coupled to a second interface, said second interface

7   operating to couple said memory card to a bus;

8   a first memory interface disposed between said

9   first interface controller and a memory block;

10   a second memory interface disposed between said

11   memory block and said second interface controller; and

12   an arbiter coupled to said first and second

13   memory interfaces for arbitrating data input operations

14   and data output operations with respect to said memory

15   block.

1   2.   The memory card as set forth in claim 1,
2   wherein said first interface comprises a network
3   interface coupled to a switch fabric disposed in a
4   telecommunications node.

1   3.   The memory card as set forth in claim 2,
2   wherein said switch fabric comprises an Ethernet fabric.

1   4.   The memory card as set forth in claim 1,
2   further comprising an error correct module coupled to
3   said memory block.

1   5.   The memory card as set forth in claim 1,
2   further comprising a synchronization logic block, said
3   synchronization logic block operating, responsive to a
4   data synchronization signal, to synchronize said data
5   input operations with respect to said memory block with
6   data input operations associated with another memory
7   card.

1   6.   The memory card as set forth in claim 1,
2 wherein said memory block comprises at least one dynamic
3 random access memory (DRAM) module.

1   7.   The memory card as set forth in claim 1,
2 wherein said memory block comprises at least one static
3 random access memory (SRAM) module.

1   8.   The memory card as set forth in claim 1,
2 wherein said memory block comprises at least one high
3 speed, high density non-volatile memory (NVM) module.

1   9.   The memory card as set forth in claim 1,
2 wherein said bus comprises a system bus operating to
3 interconnect a plurality of processor cards disposed in
4 a system shelf.

1   10.   The memory card as set forth in claim 9,
2 wherein said system bus comprises a Compact Peripheral
3 Component Interconnect (CPCI) bus.

1   11.   The memory card as set forth in claim 9,
2 wherein said system shelf forms at least a portion of a
3 telecommunications node.

1   12. A system for updating a distributed database

2   associated with a telecommunications node, comprising:

3   a database update manager for generating

4   database update signals indicative at least of updated

5   data; and

6   at least one memory card disposed in a system

7   shelf forming a portion of said telecommunications node,

8   said at least one memory card cooperating with a network

9   interface for receiving said database update signals

10   through a switch fabric, wherein said at least one memory

11   card is operable to contain at least a portion of said

12   distributed database in a memory block disposed thereon.

1   13. The system for updating a distributed database

2   associated with a telecommunications node as set forth in

3   claim 12, further comprising a synchronization signal

4   generator associated with said database update manager,

5   wherein said synchronization signal generator is operable

6   to provide a data update synchronization signal for

7   synchronizing said database update signals provided to a

8   plurality of said memory cards.

1   14. The system for updating a distributed database

2   associated with a telecommunications node as set forth in

3   claim 13, wherein said synchronization signal generator

4   is integrated with said database update manager.

1   15.   The system for updating a distributed database

2   associated with a telecommunications node as set forth in

3   claim 12, wherein said database update manager is co-

4   located with said telecommunications node.

1   16. The system for updating a distributed database

2   associated with a telecommunications node as set forth in

3   claim 12, wherein said switch fabric comprises an

4   Ethernet fabric.

1   17. The system for updating a distributed database
2 associated with a telecommunications node as set forth in
3 claim 12, wherein said memory block comprises a dynamic
4 random access memory (DRAM) module.

1   18. The system for updating a distributed database
2 associated with a telecommunications node as set forth in
3 claim 12, wherein said memory block comprises a static
4 random access memory (SRAM) module.

1   19. The system for updating a distributed database
2 associated with a telecommunications node as set forth in
3 claim 12, wherein said memory block comprises a non-
4 volatile memory (NVM) module.

1   20.   The system for updating a distributed database

2 associated with a telecommunications node as set forth in

3 claim 12, wherein said at least one memory card

4 comprises:

5   a network interface controller operable to be

6 coupled to said network interface;

7   a bus interface controller operable to be

8 coupled to a system bus interface, said system bus

9 interface operating to couple said at least one memory

10 card to a system bus;

11   first and second memory interfaces associated

12 with said memory block, wherein said first memory

13 interface is disposed between said network interface

14 controller and said memory block and said second memory

15 interface is disposed between said bus interface

16 controller and said memory block; and

17   an arbiter coupled to said first and second

18 memory interfaces for arbitrating data update operations

19 and data output operations with respect to said memory

20 block.

1   21. The system for updating a distributed database
2 associated with a telecommunications node as set forth in
3 claim 20, wherein said at least one memory card further
4 comprises an error correct module coupled to said memory
5 block.

1   22. The system for updating a distributed database
2 associated with a telecommunications node as set forth in
3 claim 20, wherein said system bus is operable to
4 interconnect a plurality of processor cards.

1   23. The system for updating a distributed database
2 associated with a telecommunications node as set forth in
3 claim 22, wherein said system bus comprises a Compact
4 Peripheral Component Interconnect (CPCI) bus.

1   24.   A telecommunications node having a distributed

2   database, comprising:

3   a database manager for generating signals

4   indicative at least one of updating and entering data

5   with respect to said distributed database;

6   a switch fabric interconnecting a plurality of

7   system shelves; and

8   a memory card disposed in each system shelf,

9   said memory card cooperating with a network interface for

10   receiving said signals through said switch fabric and

11   with a bus interface for outputting data on a system bus,

12   wherein said memory card is operable to contain at least

13   a portion of said distributed database in a memory block

14   disposed thereon.

1   25.   The   telecommunications   node   having   a
2 distributed database as set forth in claim 24, wherein
3 said switch fabric comprises an Ethernet fabric.

1   26.   The   telecommunications   node   having   a
2 distributed database as set forth in claim 24, further
3 comprising a synchronization signal generator associated
4 with said database manager, wherein said synchronization
5 signal   generator   is   operable   to   provide   a   data
6 synchronization signal for synchronizing database input
7 operations with respect to said memory cards.

1   27.   The   telecommunications   node   having a
2 distributed database as set forth in claim 24, wherein
3 said memory block comprises at least one dynamic random
4 access memory (DRAM) module.

1   28.   The   telecommunications   node   having   a
2 distributed database as set forth in claim 24, wherein
3 said memory block comprises at least one static random
4 access memory (SRAM) module.

1   29.   The   telecommunications   node   having   a
2 distributed database as set forth in claim 24, wherein
3 said memory block comprises at least one non-volatile
4 memory (NVM) module.

1   30. The telecommunications node having a

2   distributed database as set forth in claim 24, wherein

3   said system bus comprises a bus segment operating to

4   interconnect a plurality of processor cards.

1   31. The telecommunications node having a

2   distributed database as set forth in claim 30, wherein

3   said bus segment comprises a Compact Peripheral Component

4   Interconnect (CPCI) bus segment.

1   32. The telecommunications node having a

2   distributed database as set forth in claim 24, wherein

3   said memory card comprises an error correct module

4   coupled to said memory block.

1   33. The telecommunications node having a
2   distributed database as set forth in claim 24, wherein
3   said memory card comprises:
4   a network interface controller operable to be
5   coupled to said network interface;
6   a bus interface controller operable to be
7   coupled to said bus interface;
8   first and second memory interfaces associated
9   with said memory block, wherein said first memory
10   interface is disposed between said network interface
11   controller and said memory block and said second memory
12   interface is disposed between said bus interface
13   controller and said memory block; and
14   an arbiter coupled to said first and second
15   memory interfaces for arbitrating data input operations
16   and data output operations with respect to said memory
17   block.